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- 4 a) defining a phantom port containing a plurality of sequential
5 memory addresses;
6 b) generating an address to the phantom port using a conventional
7 addressing scheme;
8 c) determining an address in memory address space corresponding
9 to the generated phantom port address; and
10 d) accessing the address in memory address space.

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- 1 22. (Amended) A system for remapping between pixel coordinate
2 space and memory address space, comprising:
3 a central processing unit;
4 a frame buffer memory coupled to the central processing unit and hav-
5 ing an associated memory address scheme;
6 a memory address device coupled to the central processing unit for
7 defining a phantom port containing a plurality of sequential
8 memory addresses, each of a subset of the memory addresses
9 mapping to an address in the frame buffer memory; and
10 a remapping device coupled to the memory address device for convert-
11 ing an address between the memory address scheme of the frame
12 buffer memory and a memory address of the phantom port.

REMARKS

Claims 1-29 are pending after this amendment. Claims 1 and 22 have been amended.

The Examiner rejected claims 1-17 and 19-29 under 35 U.S.C. §103(a) as being unpatentable over Applicant's Fig. 1 in view of Nagashima or Wilde or Wang et al. This rejection is respectfully traversed.